AMENDMENTS TO THE SPECIFICATION

Kindly amend the specification as follows:

On page 1, after the heading CROSS-REFERENCE TO RELATED APPLICATION (S), kindly insert the following new paragraph:

This is a continuation of U.S. Application No. 09/776,029, entitled "Diffusion Replica Delay Circuit," filed February 2, 2001 in the names of Esin Terzioglu et al.

Please delete the second paragraph of page 2 beginning on line 6 with "Memory Module with Hierarchical Functionality," and ending on line 20 with "Attorney Docket No. 37497/B600/JFO" and substitute the following:

Memory Module ~~with~~With Hierarchical Functionality, Attorney Docket No. ~~40050/B600/JFO~~133441US02, Serial No. 09/775,477; High Precision Delay Measurement Circuit, Attorney Docket No. ~~37079/B600/JFO~~13447US02, Serial No. 09/776,262; Single Ended Sense Amplifier ~~with~~With Sample-~~and~~And-Hold Reference, Attorney Docket No. ~~37362/B600/JFO~~13435US02, Serial No. 09/776,220; Limited ~~Switch~~Swing Driver Circuit, Attorney Docket No. ~~37361/B600/JFO~~13461US02, Serial No. 09/775,478; Fast Decoder ~~with~~With Asynchronous Reset ~~with~~With Row Redundancy; Attorney Docket No. ~~37115/B600/JFO~~13451US02, Serial No. 09/775,476; Diffusion Replica Delay Circuit, Attorney Docket No. ~~37360/B600/JFO~~13454US02, Serial No. 09/776,029; Sense Amplifier ~~with~~With Offset Cancellation ~~and~~And Charge-Share Limited Swing Drivers, Attorney Docket No. ~~37363/B600/JFO~~13463US02, Serial No. 09/775,475; Memory Architecture ~~with~~With Single-Port Cell ~~and~~And Dual-Port (Read ~~and~~And Write) Functionality, Attorney Docket No. ~~37364/B600/JFO~~13464US04, Serial No. 10/173,709; Memory Redundancy Implementation, Attorney Docket No. 37496/B600/JFO13465US02, Serial No. 09/776,263; and A Circuit

Technique ~~for~~For High Speed Low Power Data Transfer Bus, Attorney Docket No. ~~37497/B600/JFO~~13459US02, Serial No. 09/776,028.

Please replace the paragraphs beginning at page 47, line 28 with "Accurate self-timed circuits ..." and ending at page 50, line 6 with "and shut-off timing signals" with the following paragraphs:

Accurate self-timed circuits are important features of robust, low-power memories. Replica bitline techniques have been described in the prior art to match the timing of control circuits and sense amplifiers to the memory cell characteristics, over wide variations in process, temperature, and operation voltage. One of the problems with some prior art schemes is that split dummy bitlines cluster word-lines together into groups, and thus only one word-line can be activated during a memory cycle. Before a subsequent activation of a word-line within the same group, the dummy bitlines must be precharged, creating an undesirable delay. The diffusion replica delay technique of the present invention substantially matches the capacitance of a dummy bitline by using a diffusion capacitor, preferably for each row. Some prior art techniques employed replica bit-columns which can add to undesirable operational delays. FIG. 20 illustrates the diffusion replica timing circuit 2000 which includes transistor 2005 with a gate lead 2015 and diffusion capacitance 2010. It is desirable that transistor 2005 be an NMOSFET transistor which, preferably, is substantially identical to an access transistor chain, if such is used in the memory cells of the memory structure (not shown). It also is desirable that the capacitance of diffusion capacitor 2010 is substantially matched to the capacitance of the associated bitline (not shown). This capacitance can be a predetermined ratio of the total bitline capacitance, with the ratio of the diffusion capacitance to total bitline capacitance remaining substantially constant over process, temperature and voltage variations. The total bitline capacitance can include both

the bitline metal and diffusion capacitances. In this fashion, all rows in a memory device which use timing circuit 2000 can be independently accessible with substantially fully-operation self-timing, even when another row in the same memory module has been activated, and is not yet precharged. Thus, write-after-read operations may be multiplexed into a memory module without substantial access time or area penalties. Thus, it is desirable to employ diffusion replica delay circuit 2000 in a memory structure such as memory structure 1800, described in FIG. 18. Diffusion replica delay circuit 2000 can be used to determine the decay time of a bitline before a sense amplifier is activated, halting the decay on the bitline. In this manner, bitline decay voltage can be limited to a relatively small magnitude, thus saving power and decreasing memory access time. Furthermore, timing circuit 2000 can be used to accurately generate many timing signals in a memory structure such as structure 1800 in FIG. 18, including, without limitation, precharge, write, and shut-off timing signals.

FIG. 21 illustrates an embodiment of the diffusion replica delay circuit 2000 in FIG. 20. Word-line activation of a memory cell frequency is pulsed to limit the voltage swing on the high capacitance bitlines, in order to minimize power consumption, particularly in wide word length memory structures. In order to accurately control the magnitude of a bitline voltage swing, dummy bitlines can be used. It is desirable that these dummy bitlines have a capacitance which is a predefined fraction of the actual bitline capacitance. In such a device, the capacitance ratio between dummy bitlines and real bitlines can affect the voltage swing on the real bitlines. In prior art devices using dummy bitlines, a global dummy bitline for a memory block having a global reset loop has been utilized. Such prior art schemes using global resetting tends to deliver pulse widths of a duration substantially equivalent to the delay of global word-line drivers. Such an extended pulse width allows for a bitline voltage swing which can be in excess of what

actually is required to activate a sense amplifier. This is undesirable in fast memory structures, because the additional, and unnecessary, voltage swing translates into a slower structure with greater power requirements. In one aspect of the present invention, dummy bitlines are preferably partitioned such that the local bitlines generally exhibit a small capacitance and a short discharge time. Word-line pulse signals of very short duration (e.g., 500 ps or less) are desirable in order to limit the bitline voltage swing. It also may be desirable to provide local reset of split dummy bitlines to provide very short word-line pulses. Replica word-line 2110 can be used to minimize the delay between activation of memory cell 2120 and related sense amplifier 2130. Such local signaling is preferred over global signal distribution on relatively long, highly capacitive word-lines. Word-line 2140 activates dummy cell 2150 along with associated memory cell 2120, which is to be accessed. Dummy cell 2150 can be part of dummy column 2160 which may be split into small groups (for example, eight or sixteen groups). The size of each split dummy group can be changed to adjust the voltage swing on the bitline. When a dummy bitline is completely discharged, reset signal [2170]2125 can be locally generated which pulls word-line 2140 substantially to ground[.]through inverter amplifiers 2135 and 2137.